FIG. 1

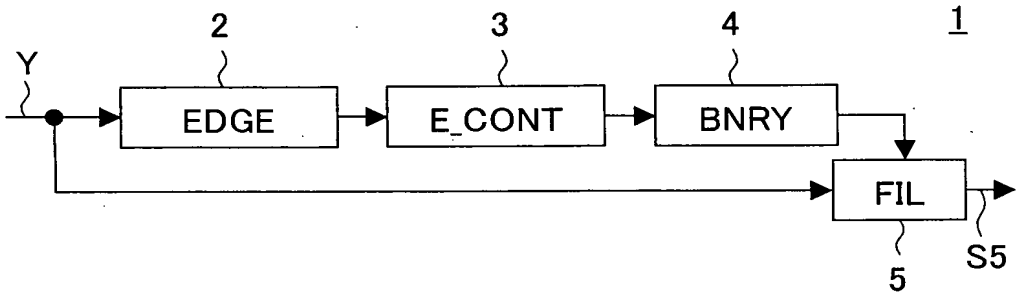

Y
2
EDGE
3
E_CONT
4
BNRY
1
FIL
5
S5

FIG. 2

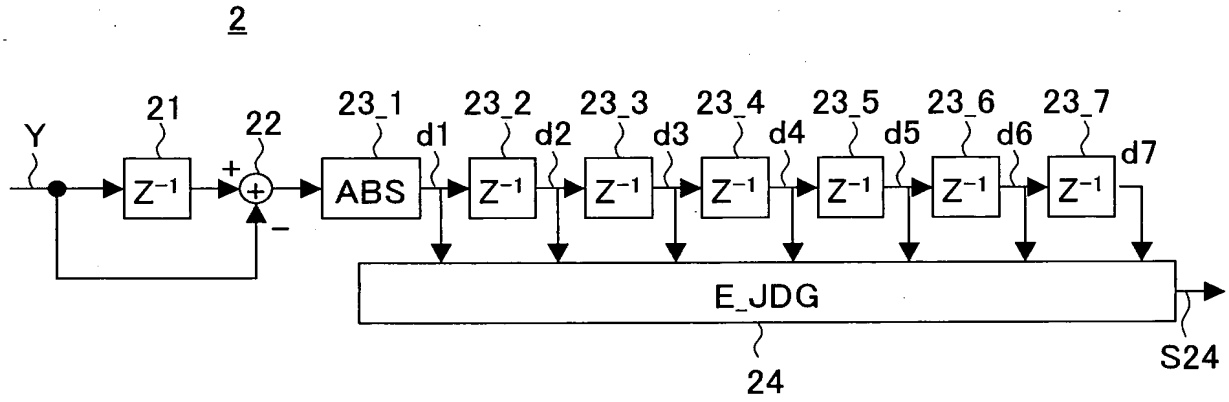

2
Y
21
Z⁻¹
22
+
−
23_1
ABS
d1
23_2
d2
23_3
d3
23_4
d4
23_5
d5
23_6
d6
23_7
d7
E_JDG
24
S24

FIG. 3

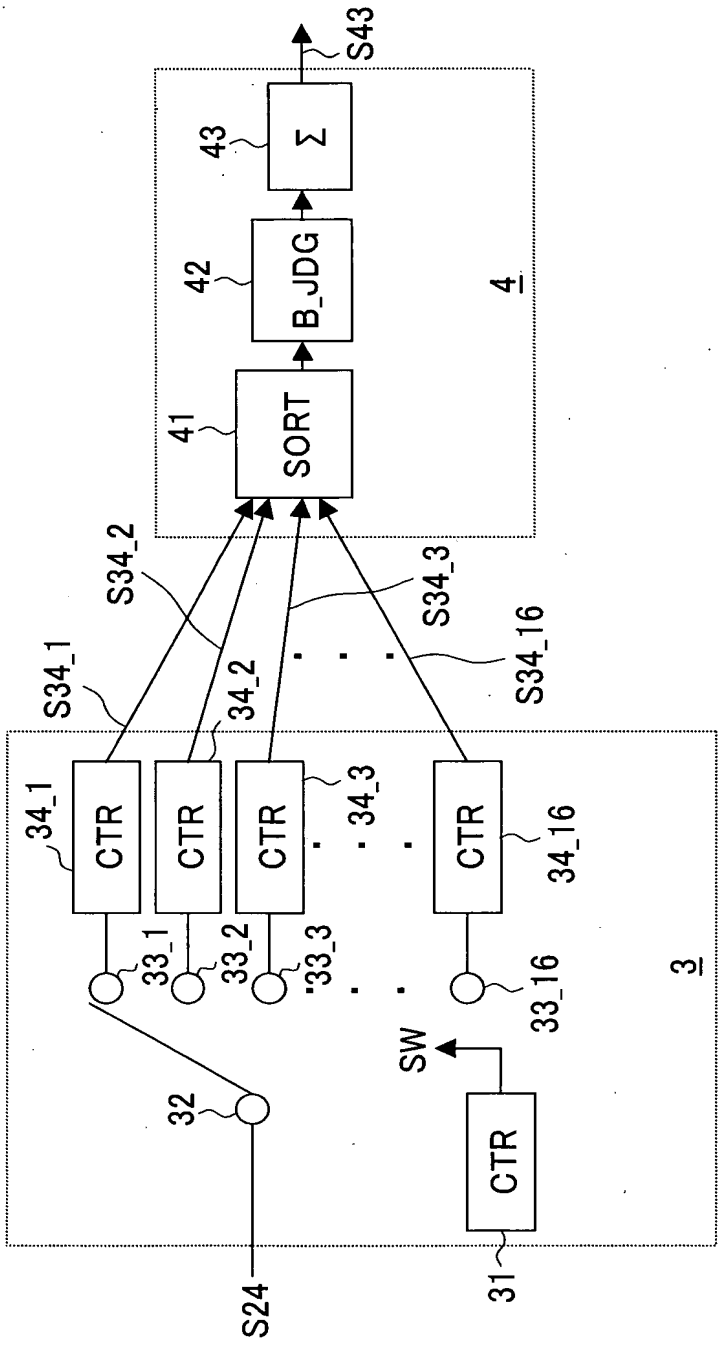

S43
43
Σ
42
B_JDG
4
41
SORT
S34_2
S34_3
S34_16
S34_1
34_2
34_1
CTR
34_3
34_16
33_1
33_2
33_3
33_16
3
SW
32
CTR
S24
31

FIG. 4

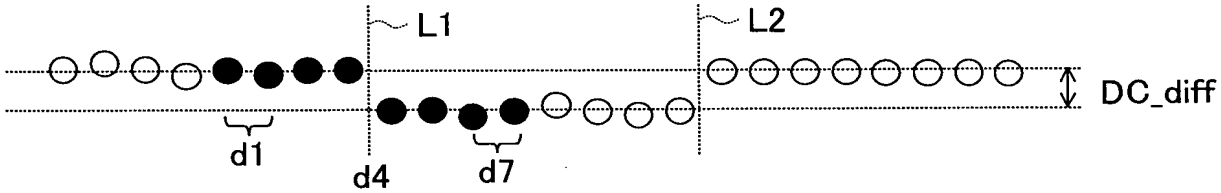


FIG. 5

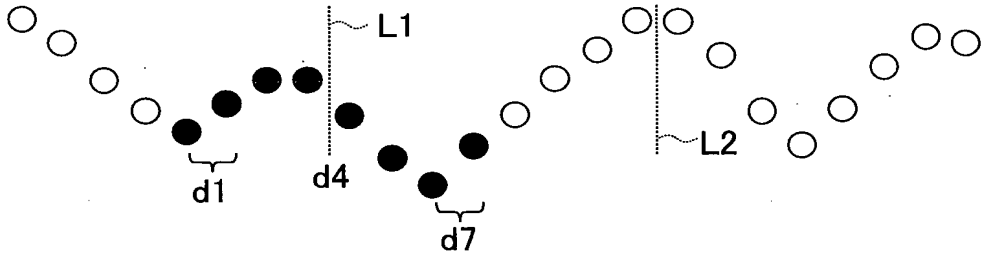


FIG. 6

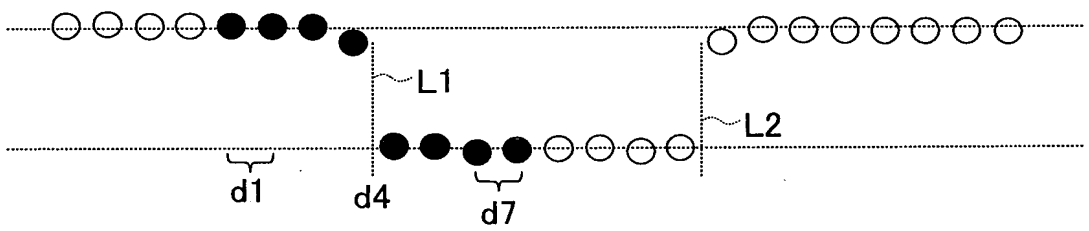


FIG. 7A CLK

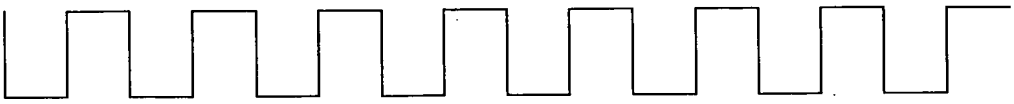


FIG. 7B H_SYNC

FIG. 7C H_CTR

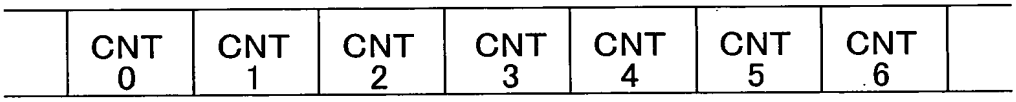


FIG. 8A CLK

FIG. 8B V_SYNC

FIG. 8C E_CTR

FIG. 8D SORT_R

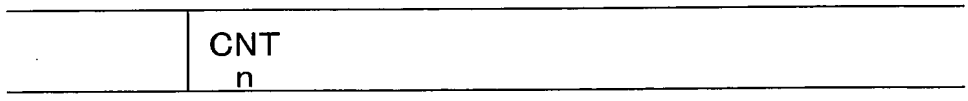


FIG. 9

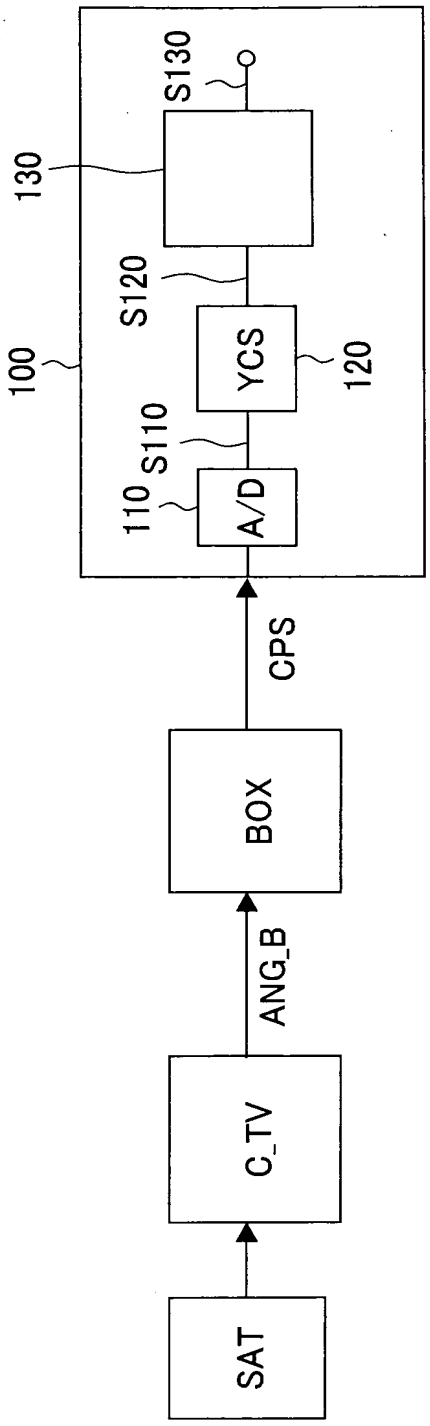
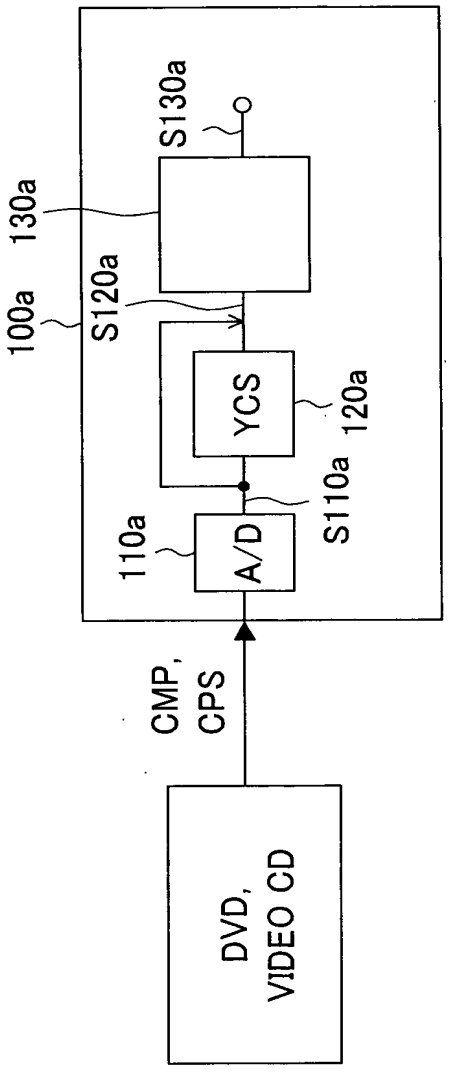


FIG. 10


DVD,
VIDEO CD
CMP,
CPS
A/D
110a
S110a
YCS
120a
S120a
100a
130a
S130a

EXPLANATION OF REFERENCES

1... block noise detection apparatus

2... edge detection circuit

21... delay circuit

22... computing circuit

23_1... computing unit

23_2 to 23_6... delay circuit

24... edge determination circuit

3... edge count circuit

31... horizontal position setting counter

32... counter switch

33_1 to 33_16... counter contact

34_1 to 34_16... edge time counter

4... boundary identification circuit

41... counter value sort unit

42... block boundary determination unit

43... time integration unit

5... filter

110, 110a... video signal processing apparatus

110, 110a... A/D converter

120, 120a... YC separator

130, 130a... block noise detector